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PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10006334	12/03/2001	438	674	2818	Q. Hoang

**APPLICANTS: Gadepally Kamesh;

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A CIP OF 09/430,348 10/29/1999 PAT 6,329,287

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☒	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	☐ yes ☐ no	NSC1-G0610 [P04402 P01]	
Verified and Acknowledged Examiners's initials			

TITLE : Method for manufacturing an integrated circuit structure with limited source salicidation

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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